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Current Carrying Capacity for Semiconductor Wire Bonds

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Introduction:

Current carrying capacity through a semiconductor device is a function of the material resistivity, thermal properties, and active area. It is technically a representation of the total power dissipation capability, as the operating voltage drop across a functional semiconductor is fixed when the device is in saturation. Theoretically, silicon dies are capable of handling a much higher current capacity than what is specified on a device datasheet. The main limiting factor in reaching the theoretical output is often related to back-end processes, such as wire bonding, packaging epoxy, and environmental operating conditions. For the purpose of this article, the proper methodology for wire bond design will be discussed, along with the direct impact on device current rating.

Determining theoretical current limitations:

For traditional single junction and bipolar junction semiconductors, there is a set potential drop across the junction of the device. This voltage drop will decrease as the junction temperature increases due to the shift in bandgap energy. Given the voltage drop and die thermal resistivity, the current rating for the die can be defined. For more complex junction technologies like the MOSFET and JFET, which maintain a low value impedance when on, a similar methodology can be used. This impedance value can be used in conjunction with die thermal resistance to define the current rating for the die. These current limits are often referred to as silicon current limits; the maximum current output the bare die can supply if packaging does not affect heat dissipation.

Determining power dissipation

$k = LT\sigma$ — *Find thermal conductivity*

$R_{th} = \frac{l}{A}k$ — *Find thermal resistance*

$P = \frac{T_J - T}{R_{th}}$ — *Find power dissipation*

For field effect transistors

$R_{DS(on)} = R_{channel} + R_{accumulation} + R_{bulk} + R_{substrate}$ — *Find total on-resistance*

$R_{DS(on)TMAX} = R_{DS(on)}(1.004)^{T_{Jmax}-T}$ — *Estimate on-resistance at junction maximum*

$I = \sqrt{\frac{P}{R_{DS(on)TMAX}}}$ — *Define silicon current limit*

For diodes and bipolar junction transistors

$V = \frac{kT}{e}\ln\left(\frac{N_D N_A}{n_i^2}\right)$ — *Find built-in voltage for all junctions*

$I = \frac{P}{V}$ — *Define silicon current limit*

Dies however, will be limited by the package they're placed in. A die will interface with the lead frame of its packaging via die attach. This interaction, along with the area and conduction properties of the lead frame material, will define the junction to lead thermal resistance of the device.

After thermal resistance is defined, the power rating of the finished device can be determined. Based on the operating junction voltage drop or impedance, the previous silicon current limit must be derated in order to meet the power rating of the finished device. This current rating will be the target specification for the final product.

$P = \frac{T_J - T_L}{R_{thJL}}$ — *Find power dissipation*

Selecting the proper bond wire:

For the device to meet the current rating outlined by its target specification, the wire bond layout has to be designed with extreme attention to detail. The three most common types of wire bond materials, gold, copper, and aluminum, all carry their own conductive properties. This is translated to a resistivity value, which, along with the length and diameter of the wire, will directly affect the performance of the finished device.

In order to ensure that the wire layout design is capable of providing the full intended current carrying capacity, a calculation can be performed to determine the overall current carrying capacity of the bond wire.

$P = kA\frac{dT}{dx} = I^2R$ *Power rating for a conductive material*

$\Delta T = \int_{T_L}^{T_J} dt = T_J - T_L$ *Define temperature delta from die to lead*

$\Delta x = \int_0^l dx = l$ *Define wire bond length*

$R = \rho\frac{l}{A}$ *Define resistance in terms of resistivity*

$A = \pi\frac{d^2}{4}$ *Define area of a wire bond*

$I = \frac{\pi d^2}{4l}\sqrt{\frac{k}{\rho}(T_J - T_L)}$ *Define wire bond current limit*

	Gold (amps)			Copper (amps)			Aluminum (amps)		
Diameter	Length			Length			Length		
mils	1	3	5	1	3	5	1	3	5
	mm	mm	mm	mm	mm	mm	mm	mm	mm
1	0.99	0.33	0.20	1.33	0.44	0.27	0.83	0.28	0.17
2	3.94	1.31	0.79	5.30	1.77	1.06	3.32	1.11	0.66
3	8.88	2.96	1.78	11.94	3.98	2.39	7.48	2.49	1.50
4	15.78	5.26	3.16	21.22	7.07	4.24	13.29	4.43	2.66
5	24.65	8.22	4.93	33.16	11.05	6.63	20.77	6.92	4.15
6	35.50	11.83	7.10	47.74	15.91	9.55	29.91	9.97	5.98
8	63.12	21.04	12.62	84.88	28.29	16.98	53.18	17.73	10.64
10	98.62	32.87	19.72	132.62	44.21	26.52	83.09	27.70	16.62

Table 1:
Current Carrying Capacity of Bond Wire

Final considerations:

After selecting the desired bond wire configuration for the device, its parasitic impact on the overall impedance of the system must be considered. This will, in-turn, lower the expected current rating of the system, which is why it is best to select a bond wire based on the target current rating prior to full assembly.

Every wire bond has a set material resistivity at room temperature, along with unique dimensional properties. These properties can be modeled as added impedance to the system. As a result, this added impedance will increase certain parasitic parameters such as forward voltage and on resistance. As dictated by Ohm's law, this means that the original target device current rating will decrease. Therefore, if the bond wire design considered the original target current rating, there will be no issues conducting the updated current rating.

$R = \rho \frac{l}{A}$	*Define resistance in terms of resistivity*
$R_{EQ} = R_{Lead} + R_{Wire} + R_{Frame} + \frac{V_{F(Die)}}{I}$	*Equivalent resistance of a packaged diode*
$R_{EQ} = R_{CE\ Lead} + R_{CE\ Wire} + R_{CE\ Frame} + \frac{V_{CE}}{I_C}$	*Equivalent resistance of a packaged bipolar*
$R_{EQ} = R_{DS\ Lead} + R_{DS\ Wire} + R_{DS\ Frame} + R_{DS\ (ON)}$	*Equivalent resistance of a packaged FET*

A final consideration to increase overall current carrying capacity is the use of parallel bond wires. Since using a large bond wire or ribbon bond is not always a viable option depending on back-end assembly tooling, a multi-bond wire layout can be a great solution for maintaining a high current carrying capacity through the semiconductor device. This however, does come with other setbacks, such as parasitic inductance and capacitance consequences.

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